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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,848	06/02/2004	Chun-Yi Chou	12877-US-PA	3847

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
MOON, SEOKYUN	
ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
12/09/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW
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Office Action Summary	Application No.	Applicant(s)	
	10/709,848	CHOU, CHUN-YI	
	Examiner	Art Unit	
	SEOKYUN MOON	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-35 and 37-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-35 and 37-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The Applicant's arguments filed on August 25, 2008 have been fully considered.

The Applicant argued [Remarks: pg 4 1st paragraph] that, in the combination of the prior arts of record ("*Kumagai*", US 2003/0218588, as modified by "*Nakano*", US 7,098,901), the driving ability of the clock signal (Kumagai: "*CLK IN*") [Kumagai: fig. 3], the display data ("*DATA IN*"), and the control signal ("*START IN*") are always enhanced by the "*input buffers 120, 121*, and *123*" [Kumagai: fig. 3] regardless of whether the transmitter operates in the master mode or the slave mode.

However, Examiner respectfully submits that regardless of whether the receiver, i.e. the "*input buffers 120, 121*, and *123*", enhances the clock signal, the display data, and the control signal or not, the combination of the prior arts teaches the limitation of independent claims 24 and 35 since the claims disclose the transmitter directly outputting the clock signal, the display data, and the control signal received from **the receiver** (emphasis added). In other words, the fact that the receiver enhances the driving ability of the clock signal, the display data, and the control signal is not related to the claim limitation.

The Applicant argued [Remarks: pg 4 2nd paragraph], "*... the timing control section 13b is used to generate the column electrode driving timing signal and the row electrode driving timing signal. However, Nakano does not teach or suggest the "timing control section 13b" can enhance an input signal*".

Examiner respectfully disagrees.

In the driving device of Nakano, the "*timing control section 13b*" generates the signals used to synchronize the inputted signal. In other words, the "*timing control section 13b*" is used to optimize the timing of outputting/processing the inputted signal. Since the optimized timing of outputting/processing the inputted signal enhances the driving ability of the inputted signal, the combination of the "*timing control section 13b*", "*selection 13c*", and "*data output section 13d*" of Nakano does enhance the driving ability of the input signal.

Lastly, the Applicant argued [Remarks: pg 5 3rd paragraph], "*Therefore, comparing with Kumagai in view of Nakano, the subject matter of claim 24 can produce new results*".

However, in response to the Applicant's argument that the subject matter of claim 24 produces new results, a recitation of the intended effect/result of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of producing the intended effect/result, then it meets the claim.

Furthermore, the claim does not disclose such new results differentiating the prior arts of record from the instant invention.

For the foregoing reasons, Examiner respectfully submits that the Applicant's arguments are not persuasive.

Currently, all of the rejections made in the previous Office Action are maintained.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 24-35** and **37-46** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumagai (US 2003/0218588) in view of Nakano (US 7,098,901).

As to **claim 24**, Kumagai teaches a source driver [fig. 3 and par. (0060)], receiving a clock signal ("*CLK IN*"), a display data ("*DATA IN*"), and a control signal ("*START IN*") to drive a display panel, comprising:

a receiver (a combination of "*input buffers 120*, *121*, *122*, and *123*") [fig. 3] for receiving the clock signal, the display data, and the control signal; and

a transmitter (a combination of "*counter 124*", "*clock control circuit 125*", "*data control circuit 126*", "*latch circuit 127*", and "*output buffers 128*, *129*, *130*, and *131*") [fig. 3] coupled to the receiver, wherein the transmitter enhances a driving ability of the clock signal, the display data and the control signal for use of another source driver in a next stage [par. (0103)-(0105)].

Kumagai does not teach the source driver receiving a master/slave setting signal and the transmitter of the source driver operating in one of a master mode and a slave mode in responsive to the master/slave setting signal, wherein the transmitter enhances a driving ability of the clock signal, the display data, and the control signal for use of another source driver in a next stage when the transmitter operates in the master mode and the transmitter directly outputs the clock signal, the display data, and the control signal received from the receiver for use of the another source driver in the next stage when the transmitter operates in the slave mode.

However, Nakano teaches a transmitter (a combination of "*timing control section 13b*", "*selector 13c*", and "*data output section 13d*") [fig. 4b] of a source driver of a display, which

operates in one of a master mode and a slave mode in responsive to a master/slave setting signal ("*external control signal supplied to a control terminal 13h*") [col. 14 lines 23-28], wherein the transmitter enhances a driving ability of the signal to be processed by the transmitter when the transmitter operates in a master mode [col. 14 lines 38-49] and the transmitter directly outputs the signal to be processed by the transmitter when the transmitter operates in a slave mode [col. 14 lines 50-59].

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the concept of Nakano, i.e. having a source driver capable of being operated in one of a master mode and a slave mode, wherein a transmitter included in the source driver enhances a driving ability of the signal to be processed by the source driver when the transmitter operates in a master mode and the transmitter directly outputs the signal to be processed by the source driver when the transmitter operates in a slave mode, to the source driver of Kumagai, in order to allow the source driver of Kumagai to be operated differently depending on the use of the source driver, and thus to optimize the function of the display including the source driver.

As to **claim 29**, Kumagai teaches the transmitter being TTL signal transmitter (as shown on fig. 6, the source driver processes TTL signals, and thus the transmitter of the source driver is a transmitter capable of processing TTL signals).

As to **claim 30**, Kumagai teaches the transmitter being TTL signal receiver (as shown on fig. 6, the source driver processes TTL signals, and thus the receiver of the source driver is a receiver capable of processing TTL signals).

As to **claims 25-28**, Kumagai as modified by Nakano teaches the transmitter and the receiver being a TTL signal transmitter and a TTL signal receiver, respectively, as discussed with respect to the rejections of claims 29 and 30.

Kumagai as modified by Nakano does not teach the transmitter being a voltage mode differential signal transmitter or a current mode differential signal transmitter and the receiver being a differential signal receiver.

However, since the Applicant has failed to disclose that specifying the type of the transmitter as being a voltage mode signal transmitter or a current mode signal transmitter and specifying the type of the receiver as being a differential signal receiver provides an advantage, is used for a particular purpose, or solves a stated problem, it is obvious matter of design choice to specify the type of the transmitter as a voltage mode differential signal transmitter or a current mode differential signal transmitter and the receiver as a differential signal transmitter.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use any one of a voltage mode differential signal transmitter, a current mode differential signal transmitter, and a TTL signal transmitter as the transmitter and to use any one of a differential signal receiver and a TTL signal receiver as the receiver, since any one of the listed transmitters and receivers would perform equally well at processing signals in the source driver.

As to **claim 31**, Kumagai teaches the transmitter (a combination of "*counter 124*", "*clock control circuit 125*", "*data control circuit 126*", "*latch circuit 127*", and "*output buffers 128, 129, 130,* and *131*") [fig. 3] including:

a data synchronization circuit (a combination of "*counter 124*", "*clock control circuit 125*", "*inverter 132*", "*data control circuit 126*", and "*latch circuit 127*") [fig. 3] synchronizing the clock signal, the display data, and the control signal received from the receiver [par. (0103) and (0105)]; and

a plurality of buffers ("*output buffers 128*, *129*, *130*, and *131*") [fig. 3] coupled to the data synchronization circuit, receiving the synchronized clock signal, the synchronized display data, and the synchronized control signal, enhancing the driving ability of the synchronized clock signal, the synchronized display data, and the synchronized control signal for use of the another source driver in the next stage.

As to **claim 32**, Kumagai teaches that the transmitter includes a plurality of voltage buffers ("*output buffers 128*, *129*, *130*, and *131*") [fig. 3] receiving the clock signal, the display data, and the control signal, enhancing the driving ability of the clock signal, the display data, and the control signal for use of the another source driver in the next stage [par. (0103) and (0105)].

As to **claim 34**, Kumagai as modified by Nakano does not expressly teach the display panel being a low temperature poly-silicon liquid crystal display panel.

However, the Examiner takes Official Notice that it is well known in the art to use a low temperature poly-silicon liquid crystal display panel as a display panel for a liquid crystal display.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the liquid crystal display of Kumagai as modified by Nakano to use a low temperature poly-silicon liquid crystal display panel, in order to allow the liquid crystal display

of Kumagai to be implemented in a portable electronic device, easily since a low temperature poly-silicon liquid crystal display panel is well known for being easily reduced in size.

As to **claim 33**, Kumagai as modified by Nakano does not expressly teach the display panel being a α-si liquid crystal display panel.

However, since the Applicant has failed to disclose that specifying the type of the display panel as a α-si liquid crystal display panel provides an advantage, is used for a particular purpose, or solves any stated problem, it is an obvious matter of design choice to specify the type of the display panel as being a α-si liquid crystal display panel.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use any one of a low temperature poly-silicon liquid crystal display panel and a α-si liquid crystal display panel as a display panel of a liquid crystal display since either one of the display panels would perform equally well at displaying images received from the source drivers.

As to **claim 35**, all of the claim limitations have already been discussed with respect to the rejection of claim 24 except for a flat panel display, comprising a display panel, a timing controller, a control circuit, and a plurality of source drivers.

Kumagai as modified by Nakano teaches a flat panel display (Kumagai: "*LCD*") [Kumagai: par. (0097) line 1], comprising:

a display panel (Kumagai: "*LCD panel 10*") [Kumagai: fig. 2];

a timing controller (Kumagai: means for providing "*CLK IN*", "*START IN*", and "*DATA IN*") [Kumagai: fig. 3] outputting a clock signal (Kumagai: "*CLK IN*"), a display data (Kumagai: "*DATA IN*"), and a control signal (Kumagai: "*START IN*");

a control circuit (Nakano: means for providing "*external control signal*" through "*control terminal 13h*") [Nakano: fig. 4b and col. 14 lines 38-59] outputting a plurality of master/slave setting signals (Nakano: "*external control signals*"); and

a plurality of source drivers (Kumagai: "*data driver IC 17*") [Kumagai: fig. 2], the plurality of source drivers being series-connected to be a series structure, the plurality of source drivers being coupled to the display panel [Kumagai: fig. 2], one end of the series structure being coupled to the timing controller, the plurality of source drivers receiving the clock signal (Kumagai: "*CLK IN*"), the display data (Kumagai: "*DATA IN*"), and the control signal (Kumagai: "*START IN*") to drive the display panel [Kumagai: fig. 3], each of the plurality of source drivers responsive to a corresponding one of the plurality of master/slave setting signals (Nakano: "*external control signal*") determining whether to enhance a driving ability of the clock signal, the display data, and the control signal for use of another source driver in a next stage [Nakano: col. 14 lines 38-59].

As to **claim 37**, all of the claim limitations have already been discussed with respect to the rejection of claim 25.

As to **claim 38**, all of the claim limitations have already been discussed with respect to the rejection of claim 26.

As to **claim 39**, all of the claim limitations have already been discussed with respect to the rejection of claim 27.

As to **claim 40**, all of the claim limitations have already been discussed with respect to the rejection of claim 28.

As to **claim 41**, all of the claim limitations have already been discussed with respect to the rejection of claim 29.

As to **claim 42**, all of the claim limitations have already been discussed with respect to the rejection of claim 30.

As to **claim 43**, all of the claim limitations have already been discussed with respect to the rejection of claim 31.

As to **claim 44**, all of the claim limitations have already been discussed with respect to the rejection of claim 32.

As to **claim 45**, all of the claim limitations have already been discussed with respect to the rejection of claim 33.

As to **claim 46**, all of the claim limitations have already been discussed with respect to the rejection of claim 34.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SEOKYUN MOON whose telephone number is (571)272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 24, 2008
/S. M./
Examiner, Art Unit 2629

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629